**What is claimed is:**

1. A read-only memory cell, comprising:

a substrate;

a plurality of bit lines, formed near the surface of the substrate;

a plurality of bit line oxides, disposed over the bit lines;

a gate dielectric layer, disposed over the substrate between the bit lines, the gate dielectric layer comprising a silicon-rich oxide layer; and

a word line, disposed over the bit line oxides and the gate dielectric layer.

2. The cell as claimed in claim 1, wherein the gate dielectric layer further comprises a first gate oxide layer, disposed between the silicon-rich oxide layer and the substrate.

3. The cell as claimed in claim 1, wherein the gate dielectric layer further comprises a second gate oxide layer, disposed between the silicon-rich oxide layer and the bit lines.

4. The cell as claimed in claim 1, wherein the silicon-rich oxide layer is <u>further</u> disposed between the word line and the bit line oxides.

5. A method for fabricating a read-only memory cell, comprising the steps of:

providing a substrate;

forming a first gate oxide layer on the substrate;

defining a bit line pattern in the first gate oxide layer and forming a plurality of bit line openings;

forming a plurality of doping areas in the substrate near its surface in the bit line openings as bit lines;

forming a plurality of bit line oxides in the bit lines;

forming a silicon-rich oxide layer over the first gate oxide layer;

forming a second gate oxide layer on the silicon-rich oxide layer; and

forming a conductive layer over the second gate oxide layer and the bit line oxides.

6. The method as claimed in claim 5, wherein the first gate oxide layer is formed by thermal oxidation.

7. The method as claimed in claim 5, wherein the first gate oxide layer is formed by chemical vapor deposition.

8. The method as claimed in claim 5, wherein the doping area is formed by phosphorus ion implantation.

9. The method as claimed in claim 5, wherein the silicon-rich oxide layer is formed by plasma chemical vapor deposition.

10. The method as claimed in claim 9, wherein the plasma chemical vapor deposition uses Tetraethylorthosilicate (TOES) as precursor.

11. The method as claimed in claim 9, wherein the plasma chemical vapor deposition uses $SiH_4$ as precursor.

12. The method as claimed in claim 5, wherein the second gate oxide layer is formed by chemical vapor deposition.